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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,150	11/13/2003	Todd A. Merritt	2008.001982	8235

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EXAMINER	
TORRES, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/712,150	MERRITT ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31,32 and 38-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31,32 and 38-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. In view of the amendment filed 08/25/2005, the examiner withdraws all previous objections to the claims.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 31, 32, 38-54 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 31 and 38 recite, "at least two of said plurality of data lines are latched from two respective memory portions". It is not clear what "respective memory portions" since claims 1 and 38 only indicate that the plurality of data lines are part of the memory device and never indicates that different portions of the memory device have their own data lines and "respective" is a relative term requiring a prior indication of memory components being related to some other element.

The Examiner assumes --at least two of said plurality of data lines are latched from two memory portions--, which is the most reasonable interpretation.

Response to Arguments

3. The Examiner summarizes the current rejection of claim 31 below, before addressing any of the Applicant's argument:

Bunker (US 6311299 B1) teaches latching data present on at least a subset of the plurality of data lines I/01-I/08 for each of the Arrays A1-A8 in Figure 2 of Bunker based upon a test mode enable signal TM (Helper Flip-Flops HFF1-HFF8 and Buffers BUF1-BUF8 in each of the Data Masking Circuits DM1-DM8 in Figure 2 of Bunker are a plurality to data latches used for latching data present on at least a subset of the plurality of data lines I/01-I/08 for each of the Arrays A_1-A_8 based upon an enable signal; Note: col. 4, lines 45-51 teach DQM0-DQM7 and MR1-MR8 signals in Data Masking Circuits DM1-DM8 are used to activate Buffers BUF1-BUF8 for read/write operations during testing by providing active low $\overline{M1} - \overline{M8}$ enable signals; col. 5, lines 58-67 in bunker teach that a test mode signal TM is used to activate the DQM0-DQM7 and MR1-MR8 signals in Data Masking Circuits DM1-DM8, which in turn are used to provide an active low $\overline{M1} - \overline{M8}$ enable signals; hence Bunker explicitly teaches latching data present on at least a subset of the plurality of data lines I/01-I/08 for each of the Arrays A1-A8 based upon test mode enable signal TM), wherein at least two of said plurality of data lines I/01-I/08 for each of the Arrays A1-A8 are latched from two respective memory portions A_1-A_8 (each of the memory arrays A_1-A_8 has its own respective I/O lines I/01-I/08; hence, for example, I/01 data lines from each of the memory arrays A_1-A_8 are latched from respective memory arrays A_1-A_8);

masking the latched data from said at least two of said plurality of data lines (the MR1-MR8 signals in the Data Masking Circuits DM1-DM8 are masking signals for masking the latched data from said plurality of data lines I/01-I/08 for respective memory arrays A_1-A_8);

compressing the masked data to determine if the masked data matches a predetermined pattern using a compressing circuit (the abstract in Bunker explicitly teaches that each of the masked data signals from each of the activated buffers BUF1-BUF8 in each of the Data Masking Circuits DM1-DM8 applied on its respective input is compared on to an expected value by the compression circuit DC1-DC8 in Figure 2 to produce a compressed error signal [E1, E2,...,E8]; Note: the individual Data Compression Circuits DC1-DC8 in Figure 2 are also a circuit since any group of circuits electrically connected form a circuit in and of themselves and in fact since 204 is an embedded memory it is a semiconductor circuit with various sub-circuits disposed inside the single embedded memory semiconductor; Note: the Expected values for each of the masked data signals are a pattern representing the expected values for the masked memory data); and providing at least a pass signal if the masked data matches the predetermined pattern (col. 2, lines 50-53 in Bunker teach compressed error signal [E1, E2,...,E8] are a pass signal enabling test circuitry to operate in a second mode; Note: if the masked signal des not match the predetermined pattern comprising expected values, then it matches an erroneous pattern; hence Bunker provides a pass signal [E1, E2,...,E8], if the masked data matches an erroneous unexpected pattern).

4. Applicant's arguments filed 08/25/2005 have been fully considered but they are not persuasive.

The Applicant contends, "Bunker discloses a system where each memory array (A1-A8) corresponds with a particular data compression circuit (DC1-DC8). In other words, Bunker discloses that data from each memory array must be compressed by a separate, corresponding compression circuit".

The Examiner disagrees and asserts that data is compressed by the compression circuit comprising the sub-circuits DC1-DC8 in Figure 2, each of the sub-circuits is connected to one of the I/O lines for each memory array (A1-A8), for example; I/O1 from each memory array (A1-A8) is connected to sub-circuit DC8 and all of the sub-circuits DC1-DC8 are required and act as a unit to process all of the I/O lines from memory array (A1-A8) and are disposed on the single embedded-memory semiconductor circuit as a single compression unit. The compression circuits DC1-DC8 in Figure 2 cannot be used separately for a single memory portion in any meaningful way since they require data from all of the memory portions (A1-A8). One of ordinary skill in the art at the time the invention was made would recognize that any group of circuits or sub-circuits that are electrically connected forms a circuit. By the dictionary definition and by what one of ordinary skill in the art at the time the invention was made would expect the circuit comprising sub-circuits DC1-DC8 in Figure 2 is still a circuit and it is a compression circuit.

The Applicant contends, "Various advantages provided by the method in claim 31 is described in the specification, which includes but is not limited to, allowing a compression to be shared by a plurality of memory portion, e.g., memory core, allowing for ease of re-design of memory, e.g,, increasing memory density without adding additional compressing circuit. See for example, page 12, lines 5-15 of the Specification. These advantages would not be available in the system disclosed in Bunker". Each of the compression circuits DC1-DC8 in Figure 2 are shared devices shared by all of the memory portions (A1-A8). Furthermore; the composite compression circuit comprising the sub-circuits DC1-DC8 in Figure 2 is a shared device. The Bottom line is the composite compression circuit comprising the sub-circuits DC1-DC8 in Figure 2 is still a compression circuit.

The Applicant contends, "The system in Bunker clearly describes that each memory portion requires a corresponding compression circuit".

The Applicant's contention is absurd. The sub-circuits DC1-DC8 in Figure 2 correspond to I/O lines from all of the Arrays (A1-A8). There is no conceivable correspondence between arrays sub-circuits DC1-DC8 since A1 corresponds to DC3 just as much as A5corresponds to DC3, they both correspond to DC3 since the I/O6 line of both A1 and A5 are electrically connected to DC3. In fact, all of the I/O6 lines of all of the memory portions are electrically connected to DC3.

The Applicant contends, "The masking function disclosed by Bunker merely receives an array of data for each masking circuit, wherein one or more of the data lines called for by claim 31 of the present invention, is masked based upon an enable signal. Therefore, the disclosure of Bunker does not read upon all of the elements of claim 31" That is also incorrect. Helper Flip-Flops HFF1-HFF8 and Buffers BUF1-BUF8 in each of the Data Masking Circuits DM1-DM8 in Figure 2 of Bunker are a plurality to data latches used for latching data present on at least a subset of the plurality of data lines I/01-I/08 for each of the Arrays A_1-A_8 based upon a test mode enable signal TM. Note: col. 4, lines 45-51 teach DQM0-DQM7 and MR1-MR8 signals in Data Masking Circuits DM1-DM8 are used to activate Buffers BUF1-BUF8 for read/write operations during testing by providing active low $\overline{M1} - \overline{M8}$ enable signals; col. 5, lines 58-67 in bunker teach that a test mode signal TM is used to activate the DQM0-DQM7 and MR1-MR8 signals in Data Masking Circuits DM1-DM8, which in turn are used to provide an active low $\overline{M1} - \overline{M8}$ enable signals; hence Bunker explicitly teaches latching data present on at least a subset of the plurality of data lines I/01-I/08 for each of the Arrays A1-A8 based upon test mode enable signal TM.

The Applicant contends, "Bunker discloses that if any of the applied read data bits applied to the compensation compression circuit DC1-DCB, has a binary value different from that of the other applied data bits, the error signal is generated".
While that may be true, col. 5, lines 54-57 in Bunker also teach that "the data compression circuits DC1-DC8 may include circuitry to compare each of the applied

read data bits to a corresponding predetermined value", which Bunker refers to as an expected value in the Abstract of Bunker. One of ordinary skill in the art at the time the invention was made would have recognized the sequence of expected values corresponding to the I/O lines is a pattern referred to as a test pattern in the art since it is a pattern used for testing the embedded memory.

The Applicant contends, "the compression circuit called for by claim 31 of the present invention calls for detecting a predetermined pattern on a subset of data lines and to provide a pass signal when the predetermined pattern is detected on the subset of data lines".

The Examiner disagrees and asserts that Bunker teaches compressing the masked data to determine if the masked data matches a predetermined pattern using a compressing circuit (the abstract in Bunker explicitly teaches that each of the masked data signals from each of the activated buffers BUF1-BUF8 in each of the Data Masking Circuits DM1-DM8 applied on its respective input is compared on to an expected value by the compression circuit DC1-DC8 in Figure 2 to produce a compressed error signal [E1, E2,...,E8]; Note: the individual Data Compression Circuits DC1-DC8 in Figure 2 are also a circuit since any group of circuits electrically connected form a circuit in and of themselves and in fact since 204 is an embedded memory it is a semiconductor circuit with various sub-circuits disposed inside the single embedded memory semiconductor; Note: the Expected values for each of the masked data signals are a pattern representing the expected values for the masked memory data); and providing at least a

pass signal if the masked data matches the predetermined pattern (col. 2, lines 50-53 in Bunker teach compressed error signal [E1, E2,...,E8] are a pass signal enabling test circuitry to operate in a second mode; Note: if the masked signal des not match the predetermined pattern comprising expected values, then it matches an erroneous pattern; hence Bunker provides a pass signal [E1, E2,...,E8], if the masked data matches an erroneous unexpected pattern).

The Applicant contends, "claim 31 calls for detecting a predetermined pattern on a subset of data lines to determine whether a pass signal is to be provided based upon comparison to a predetermined pattern".
That is incorrect. Claim 31 calls for detecting a predetermined pattern on **at least a** subset of data lines.

The Applicant contends, "The Examiner cites column 5, lines 54-57 in Bunker to assert that it teaches that the masked data is compressed within the compression circuit DC1-DCB by comparing each of the applied read mask bits to a predetermined value to determine if the applied read matches the predetermined value. However, Applicants respectfully assert that column 5, lines 54-57, discloses that the data compression circuits may include circuitry to compare each of the applied read data bits to a corresponding predetermined value, which, may then be used to generate an error signal. However, Bunker does not disclose compressing the mask data to determine if the mask data matches the predetermined pattern.

Col. 5, lines 54-57 in Bunker also teach that "the data compression circuits DC1-DC8 may include circuitry to compare each of the applied read data bits to a corresponding predetermined value", which Bunker refers to as an expected value in the Abstract of Bunker. The Abstract in Bunker teaches that the expected values are compared. One of ordinary skill in the art at the time the invention was made would have recognized the sequence of expected values corresponding to the I/O lines is a pattern referred to as a test pattern in the art since it is a pattern used for testing the embedded memory and if the masked signal des not match the predetermined pattern comprising expected values, then it matches an erroneous pattern; hence Bunker provides a pass signal [E1, E2,...,E8], if the masked data matches an erroneous unexpected pattern.

The Applicant contends, "Bunker seems to indicate the opposite of compressing the masked data, as called for by claim 31 of the present invention, since Bunker discloses compressing the unmasked bit".

The compression circuit DC1-DC8 only receives masked data. One of ordinary skill in the art at the time the invention was made would have recognized that masked data is original with various bit masked or removed from the data. The Applicant is arguing nonsense for the sake of arguing in the hopes of creating confusion about what is and what isn't. In fact, [E1, E2,...,E8] is a compressed mask signal.

The Examiner disagrees with the applicant and maintains all rejections of claims 31, 32 and 38-54. All amendments and arguments by the applicant have been considered. It

is the Examiner's conclusion that claims 31, 32 and 38-54 are not patentably distinct or non-obvious over the prior art of record in view of the reference, Bunker; Layne G. (US 6311299 B1; hereafter referred to as Bunker) as applied in the last office action, filed 07/13/2004. Therefore, the rejection is maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (f) he did not himself invent the subject matter sought to be patented.

5. Claims 31, 32 and 38-54 are rejected under 35 U.S.C. 102(e) as being anticipated by Bunker; Layne G. (US 6311299 B1; hereafter referred to as Bunker) The applied reference has a common Assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

See the Non-Final Action filed 07/13/2004 for detailed action of prior rejections.

6. Claims 31, 32 and 38-54 are rejected under 35 U.S.C. 102(f) because the applicant did not invent the claimed subject matter. Note: the subject matter of the current invention is full disclosed in Bunker; Layne G. (US 6311299 B1). See previous rejection, above.

See the Non-Final Action filed 07/13/2004 for detailed action of prior rejections.

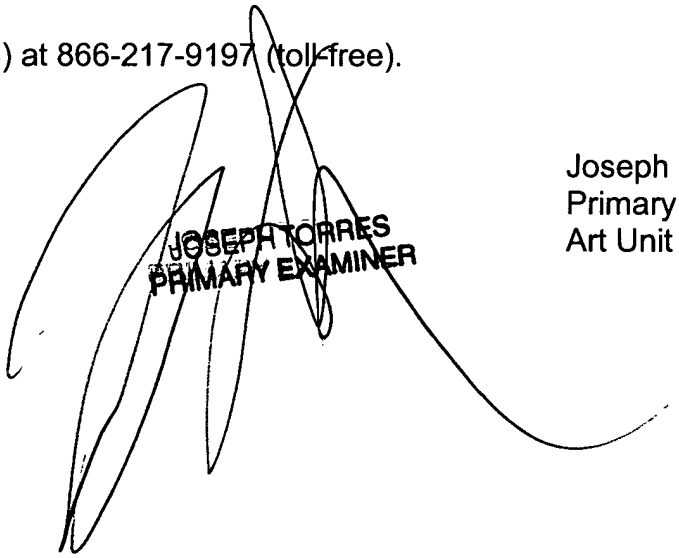
Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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